R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a method of verifying a repair of a design. The method generally comprising the steps of, (A) generating an enumeration of a plurality of fuses in the design, (B) compiling data for each of the fuses, wherein the data comprises simulation path data, and (C) simulating the design with at least one of the fuses programmed for the repair to verify the repair.

SUPPORT FOR THE CLAIM AMENDMENTS AND NEW CLAIMS

Support for the claim amendments and new claims can be found, for example in the specification on page 9 lines 15-19, page 10 lines 9-11, page 11 lines 1-3, page 11 lines 9-11, page 12 lines 12-13, page 13 lines 16-18, page 14 lines 1-4, FIGS. 1-3, and claims 1 and 12 as originally filed. Thus, no new matter has been added.

SUPPORT FOR THE SPECIFICATION AMENDMENTS

Support for the specification amendments can be found, for example in the specification on page 9 lines 20-21, page 10 lines 14-15, page 12 lines 11-14, FIGS. 1-3, and claims 7 and 12 as originally filed. Thus, no new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the specification has been obviated by appropriate amendment and should be withdrawn.

DRAWINGS-ALTERNATIVE BLOCK DIAGRAMS

The objection to the brief descriptions of FIGS. 2 and 3 has been obviated by appropriate amendment and should be withdrawn.

DRAWINGS-REFERENCE CHARACTERS

The objection to the "repair block 120" and "repair program 120" differences between the specification and FIG. 1 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 7-11 under 35 U.S.C. §112, first paragraph, has been obviated by appropriate amendment in part and is respectfully traversed in part and should be withdrawn.

The rejection of claims 7-11 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment in part and is respectfully traversed in part and should be withdrawn.

Applicants' representative respectfully traverses the assertion that the use of the word "may" in the specification is problematic or ambiguous. One of ordinary skill in the art would understand that some disclosed elements may be implemented (i) with

all disclosed characteristics in some embodiments and (ii) with less than all disclosed characteristics in other embodiments. Therefore, describing the elements using permissive language instead of mandatory language is a logical and appropriate method to inform those skilled in the art that variations to the disclosed embodiments may remain within the spirit and scope of the invention. Furthermore, the term "may" is not used in the claims, therefore, the claims are not indefinite for using permissive language.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 4, 5, 6, 12 and 13 under 35 U.S.C. §102(e) as being anticipated by Sample et al. '967 (hereafter Sample) has been obviated by appropriate amendment in part and is respectfully traversed in part and should be withdrawn.

Sample discloses a method and apparatus for design verification using emulation and simulation (Title). Sample does not appear to disclose or suggest every element as arranged in the pending claims. As such, the pending claims are fully patentable over the cited reference and the rejection should be withdrawn.

Pending claims 1 (method), 12 (apparatus) and 13 (means) provide generating an enumeration of **a plurality of fuses in a design.** In contrast, Sample appears to be silent regarding enumerating fuses in a design. Column 1, lines 38-47 of Sample

disclose transforming a netlist of gates and flip-flops into transistor equivalents or library cells. Gates, flip-flops, transistors, transistor equivalents and library cells are not fuses. Column 1, lines 38-47 of Sample also mentions **fuses as part of a programmable device** distinguishable from the netlist design. The rest of Sample appears to be silent in terms of the fuses being part of the design manufactured using the programmable device. In particular, fuses do not appear to be mentioned anywhere else in Sample other than in column 1, lines 38-47. Therefore, Sample does not appear to disclose or suggest generating an enumeration of a plurality of fuses in a design as claimed.

Furthermore, pending claims 1, 12 and 13 provide **compiling data for each of the fuses**, wherein the data comprises simulation path data. In contrast, Sample appears to be silent about compiling simulation path data for fuses. Sample only mentions **burning fuses** for manufacturing a design with a programmable device. Sample appears to make no other references to fuses. Therefore, Sample does not appear to disclose or suggest compiling data for each of the fuses, wherein the data comprises simulation path data as presently claimed.

Furthermore, pending claims 1, 12 and 13 provide simulating the design with at least one of the fuses programmed for a repair to verify the repair. In contrast, Sample appears to be silent about repairing a design by programming a fuse. As argued

above, column 1, lines 38-47 of Sample only mentions the design being **manufactured** with a programmable device by burning fuses in the programmable device. Therefore, Sample does not appear to disclose or suggest simulating a design with at least one fuse **programmed for a repair** to verify the repair as presently claimed. As such, the pending claims are fully patentable over the cited reference and the rejection should be withdrawn.

Pending claim 4 provides a step of generating a list of layout coordinates and schematic instance paths in a design as part of a compiling. In contrast, Sample does not appear to disclose or suggest schematic instance paths. An electronic copy of Sample was downloaded from the U.S. Patent and Trademark Office web site (www.uspto.gov). A search for the term "schematic" did not find any occurrences. A search for the term "instance" only found (i) an "instance U1 and m0-m7" and (ii) an "instance line_select" (column 13, lines 22-26 of Sample). Furthermore, page 9, item 46 of the Office Action references a "netlist generator" element 140 and a "part, place, route" element 148 of Sample, but provides no evidence how the phrases"netlist generator" or "part, place, route" anticipate generating schematic instance paths. Therefore, Sample does not appear to disclose or suggest generating a list of layout coordinates and schematic instance paths in a design as part of a compiling as presently claimed. As such, the pending claim is

fully patentable over the cited reference and the rejection should be withdrawn.

Pending claim 5 provides a step of **generating a fuse report**. In contrast, column 1 lines 38-47 of Sample disclose **burning fuses** in a programmable device. Sample does not appear to make any other reference to fuses. Since burning a fuse is not the same as generating a fuse report, Sample does not appear to disclose or suggest generating a fuse report as presently claimed. As such, the pending claim is fully patentable over the cited reference and the rejection should be withdrawn.

Applicants' representative respectfully traverses the Examiner's suggestion that it is inherent to require a "fuse report" for burning fuses because fuses can be selected manually for burning. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988).

Pending claim 6 provides a step of listing physical locations of a device in a design in response to a fuse report. Page 10, item 50 of the Office Action states, "Note that burning the fuses requires listing the physical location of the fuses to be burned,...". Physical locations of **fuses in a programmable device programmed per a design** are not the same as physical locations of a **device in the design** itself. Furthermore, as argued above, Sample appears silent about a fuse report so Sample cannot disclose

or suggest burning a fuse within a design in response to a fuse report. Therefore, Sample does not appear to disclose or suggest listing physical locations of a device in a design in response to a fuse report as presently claimed. As such, the pending claim is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2, 3 and 9-11 under 35 U.S.C. §103(a) as being obvious over Sample '967 in view of Tzori '044 has been obviated by appropriate amendment in part and is respectfully traversed in part and should be withdrawn.

The rejection of claims 7 and 8 under 35 U.S.C. §103(a) as being obvious over Sample '967 in view of Tzori '044 and Higgins et al. '349 (hereafter Higgins) has been obviated by appropriate amendment in part and is respectfully traversed in part and should be withdrawn.

Tzori teaches a concurrent hardware-software co-simulation (Title). Higgins teaches built-in self-test and self-repair methods and devices for computer memories comprising a reconfigurable memory device (Title). Sample, Tzori and Higgins alone and in combination do not appear to teach or suggest every element as arranged in the pending claims. As such the pending

claims are fully patentable over the cited references and the rejection should be withdrawn.

Assuming, *arguendo*, that it would have been obvious to combine the teachings of Sample, Tzori, and Higgins (for which Applicants' representative does not necessarily agree), the resulting combination does not teach or suggest every element as arranged in pending claim 7. In particular, pending claim 7 provides generating a repair file that predicts at least one fuse programmed for a repair. However, page 13, item 66 of the Office Action states that Higgins teaches a table **listing faulty addresses**. The table of Higgins appears to point to the faults detected by a test. In contrast, the repair file of pending claim 7 **predicts at least one fuse** programmed for a repair. Listing faulty addresses does not appear to teach or suggest predicting fuses programmed for a repair. Therefore, Sample, Tzori and Higgins alone and in combination do not appear to teach or suggest generating a repair file that predicts at least one fuse programmed for a repair as presently claimed. As such, the pending claim is fully patentable over the cited references and the rejection should be withdrawn.

Assuming, *arguendo*, that it would have been obvious to combine the teachings of Sample, Tzori, and Higgins (for which Applicants' representative does not necessarily agree), the resulting combination does not teach or suggest every element as

arranged in pending claim 8. In particular, pending claim 8 provides creating a repair program in response to a repair file. In contrast, page 13, item 70 of the Office Action states that Higgins teaches that location information is supplied to a controller for a laser repair device which achieves a hardware fix. However, the Office Action and Higgins appear to be missing a connection between the claimed repair program and the claimed repair file. If the location information taught by Higgins is the claimed repair program, there is no indication in Higgins that the location information is created in response to a repair file. If the location information taught by Higgins is the claimed repair file, the step of creating a repair program in response to the location information appears to be missing from Higgins. Therefore, Sample, Tzori and Higgins alone and in combination do not appear to teach or suggest creating a repair program in response to a repair file as presently claimed. As such, the pending claim is fully patentable over the cited references and the rejection should be withdrawn.

Assuming, *arguendo*, that it would have been obvious to combine the teachings of Sample and Tzori (for which Applicants' representative does not necessarily agree), the resulting combination does not teach or suggest every element as arranged in pending claim 10. In particular, pending claim 10 provides a step of listing an output of a repair program as a list of coordinates

for at least one fuse programmed for a repair in terms of a plurality of logical addresses. In contrast, page 14, item 76 of the Office Action references column 1, line 44 of Sample as teaching a list or layout specification used to burn fuses. As argued above, Sample teaches burning fuses in a programmable device to manufacture a design using the programmable device. In contrast, the fuses in pending claim 10 are programmed for a repair in a design. Furthermore, the Office Action appears to be silent for how Tzori teaches or suggests listing an output of a repair program as a list of coordinates for at least one fuse programmed for a repair in terms of a plurality of logical addresses. No cites to the text or figures of Tzori appear in the rejection argument for the pending claim 10. The Examiner is therefore respectfully requested to (i) provide a clear cite to Tzori or (ii) withdraw the rejection.

Regarding pending claim 11, Applicants' representative respectfully traverses the Examiner's suggestion that it is inherent that (i) lists have coordinates necessary to locate and burn fuses and (ii) modern manufacturing system would store the list in a memory because (a) some fuses may be located through electrical connections instead of coordinates and (b) some modern manufacturing systems are believed to accept coordinates from manual entry. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts*

Package, Inc., 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). It is not certain that all lists have coordinates of fuses nor is it certain that all lists of coordinates will be stored in a memory. The Examiner is respectfully requested to either (i) provide a cite where Sample and/or Tzori teach or suggest storing coordinates in a memory as presently claimed or (ii) withdraw the rejection.

Claims 2, 3 and 7-11 depended either directly or indirectly from independent claim 1, which is now believed to be allowable. As such, the presently pending invention is fully patentable over the cited references and the rejection should be withdrawn.

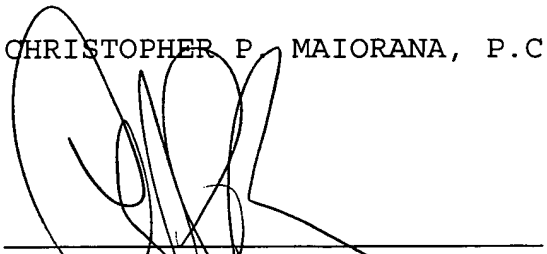
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please replace the paragraph starting on page 4, line 13 with the following paragraph:

Referring to FIG. 1, a block diagram of a method 100 is shown in accordance with a preferred embodiment of the present invention. Fuses in a design may be enumerated and data collected and stored in a file. The data may include schematic path data, verilog simulation path data and/or physical fuse location data. Multiple representations of the design and/or data may be accessible by other tools, such as netlister and/or layout versus schematic (LVS). The data may be used to enumerate the fuses. The data may be implemented in order to test and/or repair the design. References to "verilog" refer [generally] to the verilog hardware description language (HDL) as defined by the IEEE 1364-1995 standard.

Please replace the paragraphs starting on page 4, line 7 with the following paragraphs:

FIG. 2 is [an alternate] a block diagram of an example apparatus implementing the present invention; and

FIG. 3 is [another alternate block diagram of the present invention] a flow chart of an operation of the method of FIG. 1.

Please replace the paragraph starting on page 5, line 14 with the following paragraph:

The method 100 may comprise a design data block 102, a netlist block 104, a simulation block 106, a generation block 108, a table block 110, an application block 112, a program statement block 114, a location block 116, a schematic/simulation block 118, a repair program or repair block 120 and a test block 122. The generation block 108 may receive fuse data from the design data block 102. The generation block 108 may write the fuse data into a file and perform error checking on the file.

Please replace the paragraphs starting on page 9, line 10 with the following paragraphs:

Construction of the repair [block] program 120 may rely on part-specific redundancy information and errors found after a first-silicon delay part production. The repair [block] program 120 may receive the errors from the defect block 122. The repair [block] program 120 may be exercised in advance of the first-silicon for specific part failures. The repair [block] program 120 may predict fuse locations that, if programmed, may correct a part experiencing failure. The method 100 may provide an easy and

reliable method to perform simulations that emulate a design as if those locations were programmed on the die by the laser.

Referring to FIG. 2, [an alternate method 200 of] a block diagram of an example apparatus 200 implementing the present invention is shown. The [method] circuit 200 may comprise a design flow block or design flow circuit 202 and a stand-alone block or stand-alone circuit 204. The design flow block or circuit 202 may comprise a fuse network block 206, a fuse LVS block 208 and a design/database circuit 210. The fuse network block 206 and the fuse LVS block 208 may provide data to the stand-alone block or circuit 204. In one example the design/database circuit 210 may be implemented as a design flow and Opus design database.

Please replace the paragraphs starting on page 11, line 1 with the following paragraphs:

The fuse application block 220 may write one or more ASCII report files. A repair memo, also referred to as a repair file, may be manually assembled from the report files. One or more steps may be manually determined and may be incorporated into the repair memo or file. The repair memo or file may be exercised to predict coordinates to program. The coordinates may be mapped to verilog paths. Simulations of the verilog paths may be performed to verify the expected function.

The design flow [block] circuit 202 may further comprise a browse block 240. The browse block 240 may capture, in the schematic, enough knowledge of the fuses to elevate the fuses to a higher level of abstraction. The user may describe, in application terms, the desired redundancy event. For example, the redundancy event may comprise [of] replacing column C in quadrant Q. The coordinates to program may be automatically determined. However, the simulation may still be required to verify the function (e.g., to verify that the application specific knowledge captured in the schematic describing specific intent of each fuse is correct).

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) A method of [automated enumeration of one or more devices] verifying a repair of a design, comprising the steps of:

(A) generating an enumeration of a plurality of fuses in said design; [and]

(B) compiling data for each [one] of said [plurality of] fuses, wherein said data comprises [(i) one or more schematic path data, (ii) one or more] simulation path data [and/or (iii) one or more physical location data]; and

(C) simulating said design with at least one of said fuses programmed for said repair to verify said repair.

2. (AMENDED) The method according to claim 1, wherein said [one or more] simulation path data comprises verilog simulation path data.

3. (AMENDED) The method according to claim [1] 14, wherein said schematic path data comprises at least one of a schematic path [paths], a property [properties], a hierarchy [and/or] and a verilog path [paths].

4. (AMENDED) The method according to claim 1, wherein step (B) further comprises the sub-step of:

generating a list of layout coordinates and schematic instance paths in said design as part of said compiling.

5. (AMENDED) The method according to claim 1, further comprising the step of:

generating [one or more] a fuse report [reports in response to said compiling].

6. (AMENDED) The method according to claim 5, further comprising the step of:

listing physical locations of [one or more devices] a device in said design in response to said fuse report [reports].

7. (AMENDED) The method according to claim 1, further comprising the step of:

generating a repair file that predicts said at least one of said fuses programmed for said repair [in response to said compiling].

8. (AMENDED) The method according to claim 7, further comprising the step of:

creating a [laser] repair program in response to said repair file.

9. (AMENDED) The method according to claim [1] 8, further comprising the step of:

verifying a function of said design in response to said [a] repair program [with one or more simulations].

10. (AMENDED) The method according to claim [1] 8, further comprising the step of:

listing an output of said repair program as a list of coordinates [of] for said at least one of said fuses programmed for said [that need to be blown for the desired] repair in [corresponding] terms of a plurality of logical addresses.

12. (AMENDED) An apparatus comprising:

a first circuit configured to enumerate a plurality of fuses in a design; and

a second circuit configured to (i) compile data for each [one] of said [plurality of] fuses, wherein said data comprises [(i) one or more schematic path data, (ii) one or more] simulation path data [and/or (iii) one or more physical location data] and (ii) perform a simulation said design with at least one of said fuses programmed for a repair of said design to verify said repair.

13. (AMENDED) An apparatus comprising:

means for generating an enumeration of a plurality of fuses in a design; [and]

means for compiling data for each [one] of said [plurality of] fuses, wherein said data comprises [(i) one or more schematic path data, (ii) one or more] simulation path data [and/or (iii) one or more physical location data]; and

means for simulating said design with at least one of said fuses programmed for a repair of said design to verify said repair.

14. (NEW) The method according to claim 1, wherein said data further comprises schematic path data.

15. (NEW) The method according to claim 1, wherein said data further comprises physical location data.

16. (NEW) The method according to claim 1, further comprising the step of:

mapping a plurality of co-ordinates of said fuses to a plurality of verilog program statements.

17. (NEW) The method according to claim 8, further comprising the step of:

checking said repair file and said repair program for an error.

18. (NEW) The apparatus according to claim 12, wherein said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design.

19. (NEW) The apparatus according to claim 12, wherein said first circuit is further configured to collect data relevant to said fuses that are grouped.

20. (NEW) The apparatus according to claim 12, wherein said second circuit is further configured to write a report file.